Implementing Modal Software in Data Flow for Heterogeneous Architectures

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Software for embedded systems is often based on distinct processing **modes**. A simple example of such modal behavior is a radar system that switches between search mode and tracking mode as targets are located. In complex software systems, the system may have dozens of modes, including sub-modes, forming a deep hierarchy. Such large embedded systems often must be implemented on boards of multiple digital signal processors (DSP). Increasingly, field programmable gate arrays (**FPGA**) are being used alongside DSPs as a method for meeting the throughput and latency requirements of these systems. Gedae is an **integrated design environment** for deployed systems and advanced demonstrators based on DSPs (e.g., AltiVec, PowerPC, TigerSHARC) or distributed networks (e.g., Linux clusters). This paper describes extensions to Gedae's language that empower developers to easily develop modal software and enable them to port that software to **heterogeneous architectures**, including a new class of boards that contain both DSPs and FPGAs.

Modal Software

Gedae's language is based on **data flow**. A flow graph implements an application, and each primitive node in the flow graph defines the data flow relationship between its inputs and outputs. The three core types of data flow relationships are

- Static: the number of tokens produced and consumed is constant and determined at application start-up.
- Dynamic: the number of tokens produced and consumed is determined at runtime, and the node cannot execute unless full input queues are ready to be processed and empty output queues are ready to be written to.
- Nondeterministic: the number of tokens produced and consumed is determined at runtime, and there are no restrictions on when the node can execute.

While these basic types of data flow are sufficient to implement any application, complex modal applications would require large amounts of application control to be implemented in an ad hoc manner alongside the signal and data processing. To reduce this overhead and provide a general solution to the problem of modal software development, the Gedae language has been extended to allow developers to mark **segments** of streams. These user-specified markers on the beginning and end of stream segments can produce side effects that alter graph behavior, such as switching to tracking mode after a target has been found in a stream of radar data.

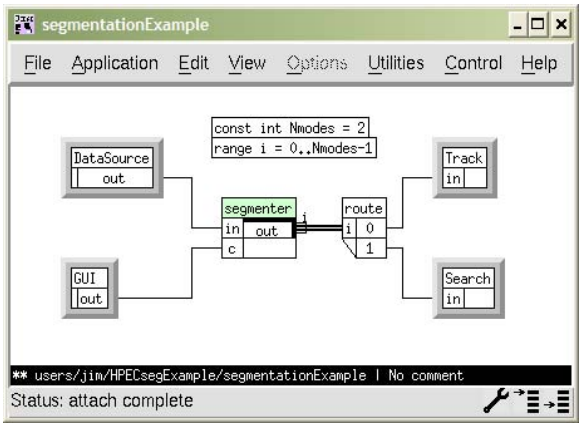

Figure 1 – Two-mode radar implemented using segmentation

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Gedae's primitive language is based on C with functional and variable-based extensions to allow the developer to interface with Gedae's data structures. This C-code is grouped into methods, e.g., the `Start` method is executed at start-up, the `Apply` method is executed when the primitive has data to process, etc. The example two-mode radar application is shown in Figure 1. Two subgraphs implement the two modes, `Track` and `Search`. The `segmenter` primitive reads data from an I/O device (`DataSource`) and a graphical user interface (`GUI`) to create two branches of data and uses the `segment()` function to place the segment markers in the streams. As the markers are encountered in downstream primitives, the `Reset` and `EndOfSegment` methods are invoked, creating side effects and forming distinct boundaries between modes.

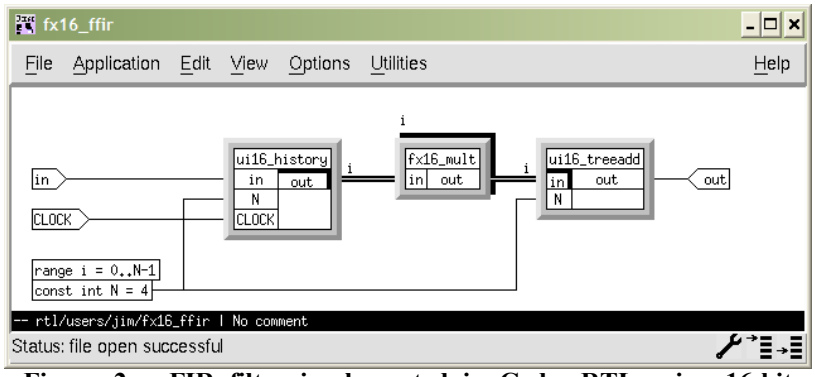

Figure 2 – FIR filter implemented in Gedae-RTL using 16-bit fixed-point arithmetic

Heterogeneity

In embedded systems, FPGAs are often used alongside DSPs to implement front-end signal processing that must be processed at a high throughput. With the increased focus on targets such as FPGAs, the Gedae block diagram language has been extended to enable porting to firmware. Unlike the AltiVec, PowerPC, and TigerSHARC, these new targets generally do not allow cross-compilation of C-code. To support other languages, Gedae has been augmented with a single sample meta-language based on the theory of register transfer languages called **Gedae-RTL**. This language is capable of exporting VHDL code for FPGAs as well as Ansi-C code optimized for a DSP.

Functionality built using Gedae-RTL uses the new single sample primitive type. Conceptually, a graph of single sample primitives forms a processing pipeline that is enabled by a clock. These single sample primitives are built upon seven fundamental functions: register, assignment, decimate, clock, memory, memory read, and memory write. The register function copies the input variable to the output with a delay of one clock pulse. The assignment evaluates an expression and assigns its value to a variable. The memory function declares a memory buffer, and the memory read and write functions access a buffer. Decimate and clock functions set and retrieve the clocks tied to variables.

Much like Gedae's core language, the Gedae-RTL graph specifies only the functionality of the graph without regard to the target or its programming language. For example, Figure 2 shows a FIR filter implemented in Gedae-RTL, built from a register pipeline (`ui16_history`), multipliers (`fx16_mult`), and a tree-adder (`ui16_treeadd`) with no target-specific processing. Through Gedae's knowledge of the target processor, a graph such as this FIR filter is transformed to generate correct results on the target and for optimized performance on the target. Then target code is exported to implement the application. Components implemented in Gedae-RTL interact seamlessly with core Gedae components, allowing an entire heterogeneous system to be specified in the Gedae programming environment.

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Abstract

Agenda

Implementing Modal Software in Data Flow for Heterogeneous Architectures

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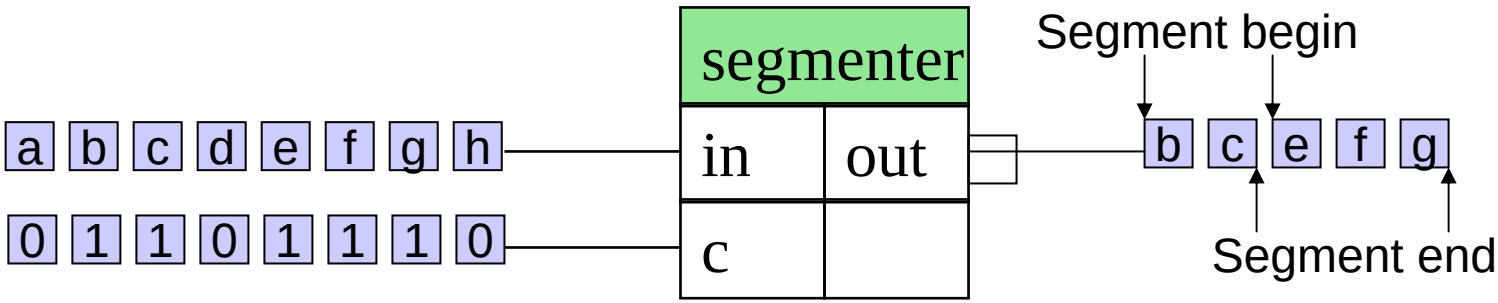
Core Gedae Data Flow

- Gedae's Core Data Flow Relationships

	Number of Tokens Produced/Consumed	Restrictions on Execution
static	Preplanned	Full Inputs/Empty Outputs
dynamic	Determined at Runtime	Full Inputs/Empty Outputs
nondet	Determined at Runtime	None

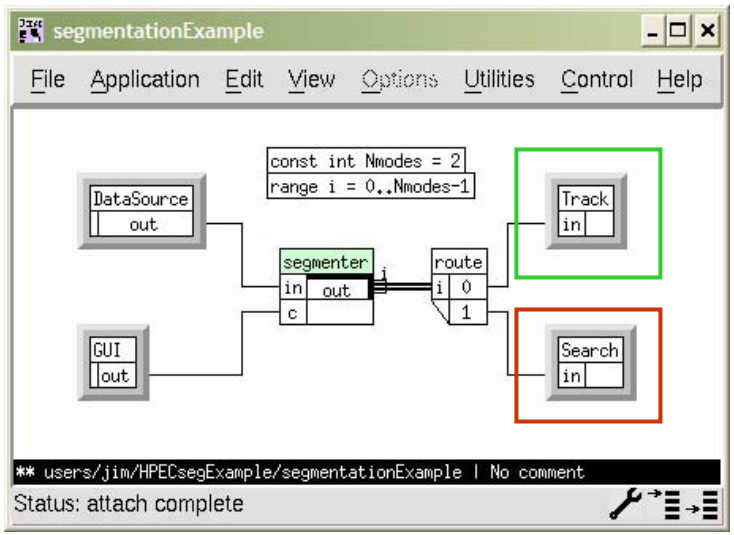
- Any application control can be implemented but
  - Complex modal software requires lots of logic
  - Done in an ad hoc manner that isn't reusable

Stream Segmentation

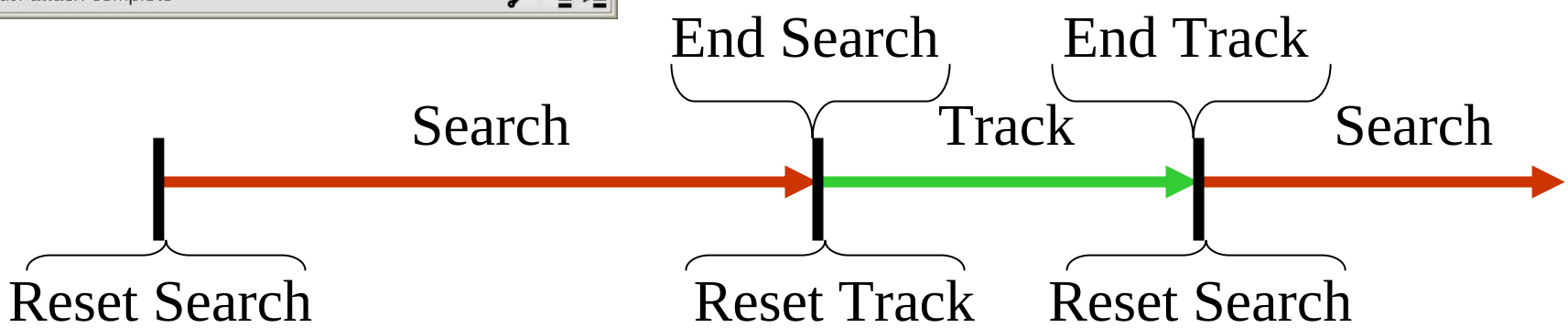


- Infinite streams can be broken into finite length segments
- Segments are processed independently
- Primitives add segment begin and end markers to a data stream
- Each marker causes side effects downstream

Using Segmentation to Control Modes

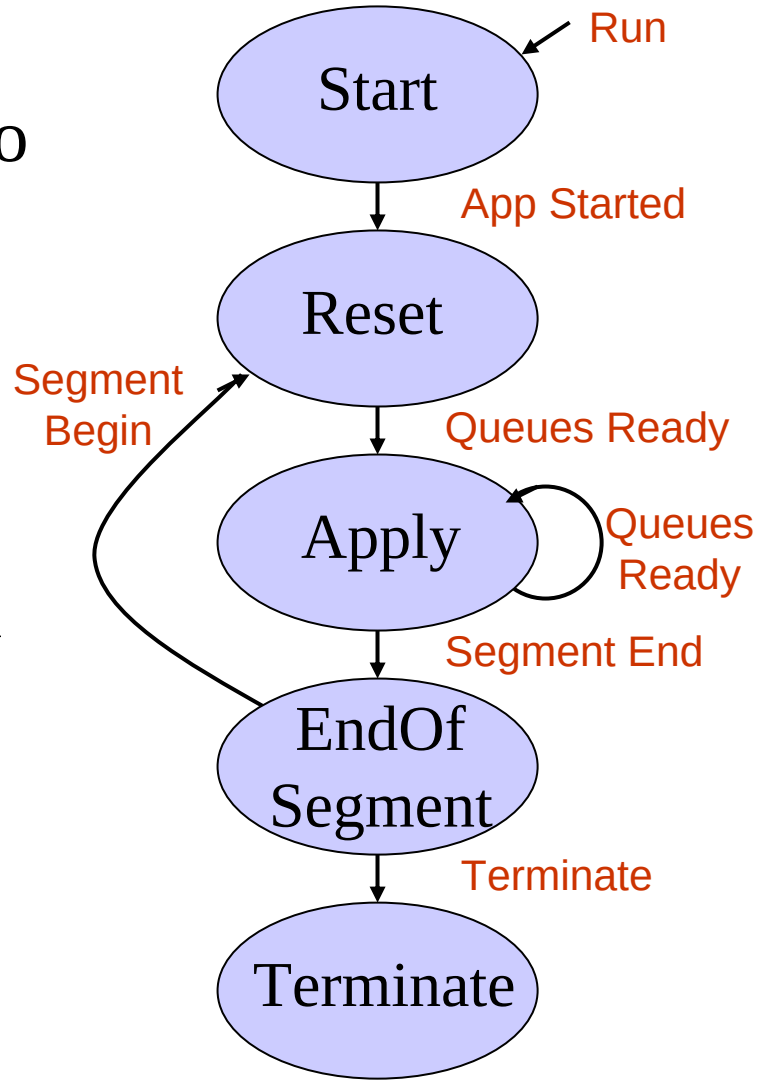


- Segment markers cause old mode to end and new one to reset
- Exclusivity allows memory sharing between modes

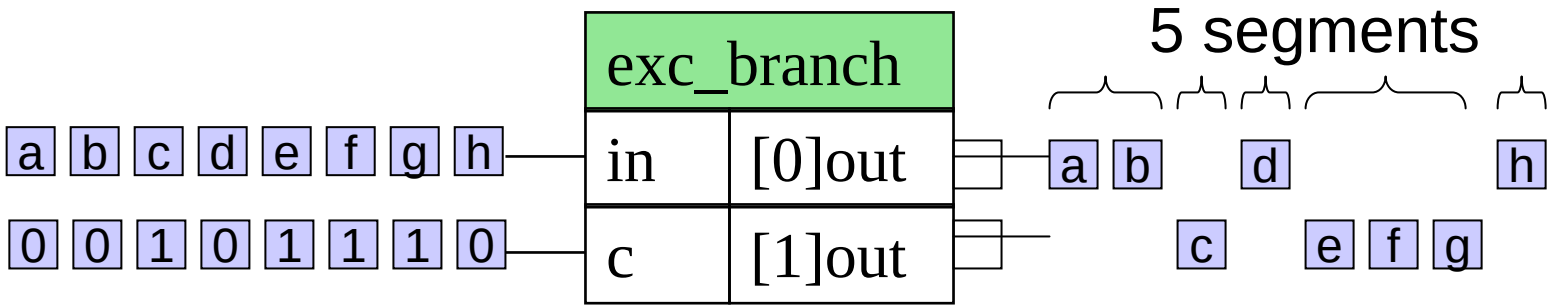


Reset and EndOfSegment Methods

- Primitive code is grouped into methods
- When methods are executed:
  - Start: Beginning of execution
  - Reset: Beginning of each segment (start mode)
  - Apply: When queues are ready for execution (execute mode)
  - EndOfSegment: End of each segment (end mode)
  - Terminate: End of execution

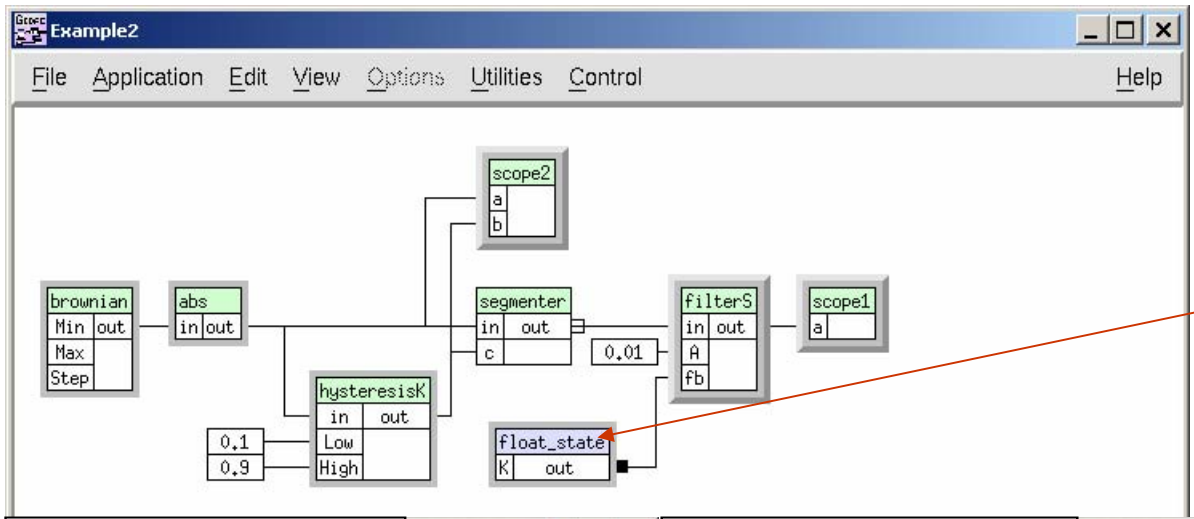


Sharing Resources Between Modes



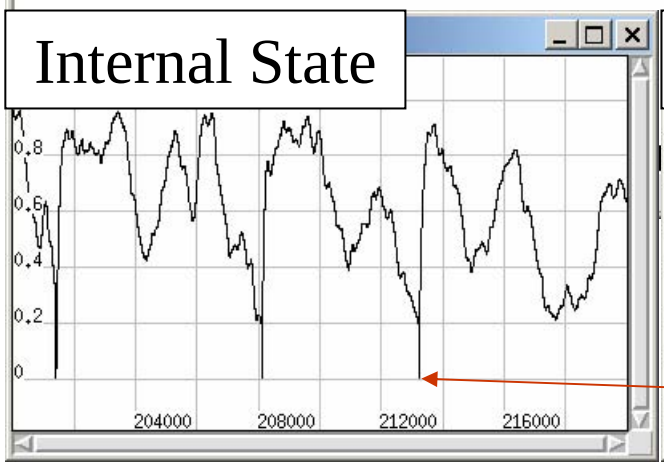
- Exclusivity: Only one output is actively producing a segment at any given time
- Subgraphs controlled by a family of exclusive outputs can share resources
  - Schedule memory
  - Queue memory
  - State variables

Sharing State Information Between Modes

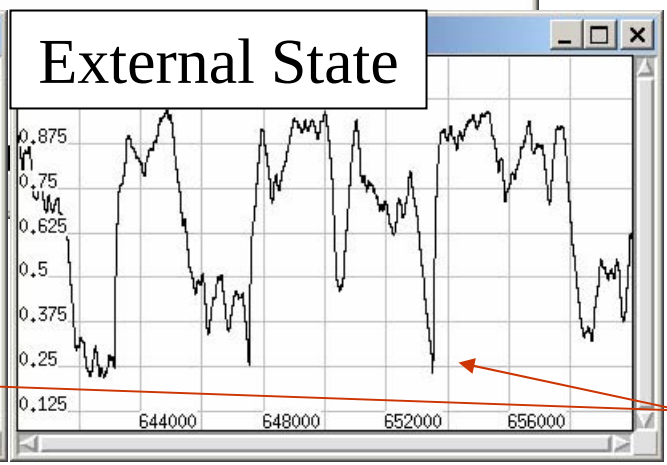


Moving static variable out of `filterS` subgraph causes it to be persistent between segment boundaries

Internal State



External State

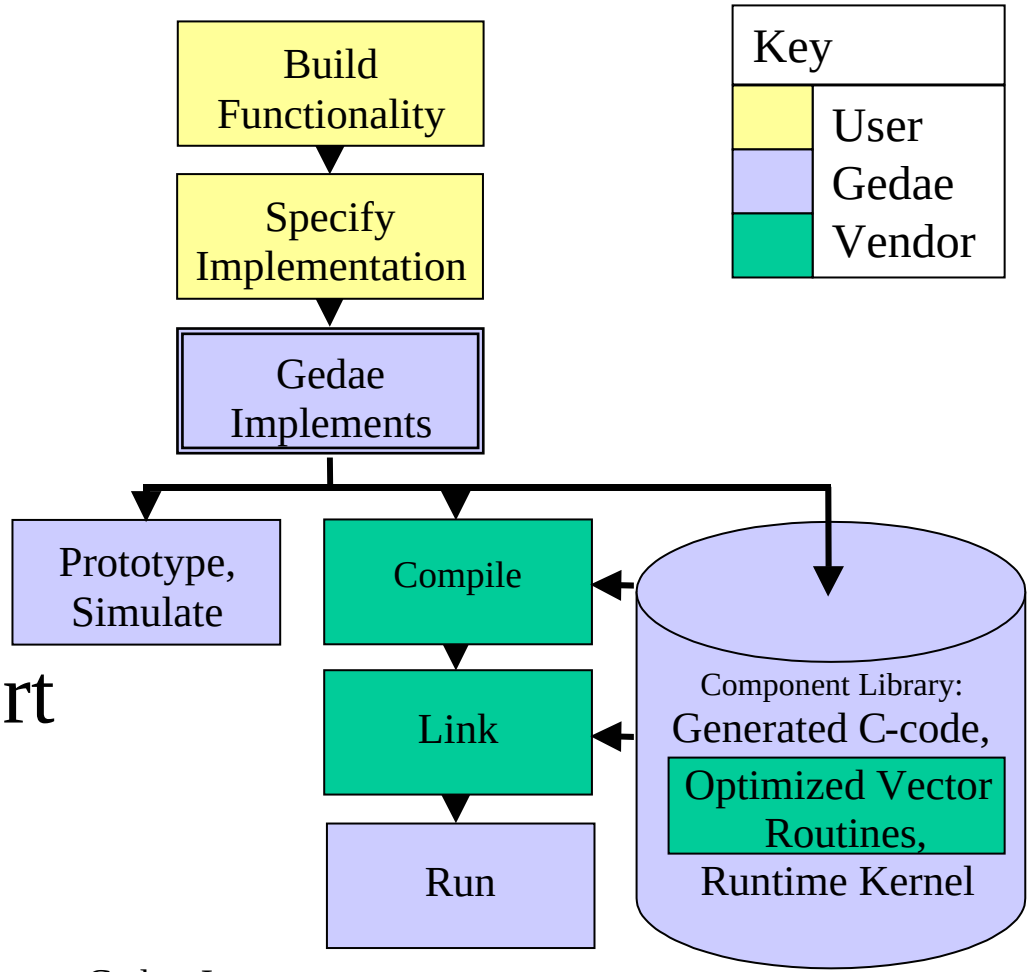


No transients due to clearing of static variables at segment boundaries

Moving to Heterogeneity

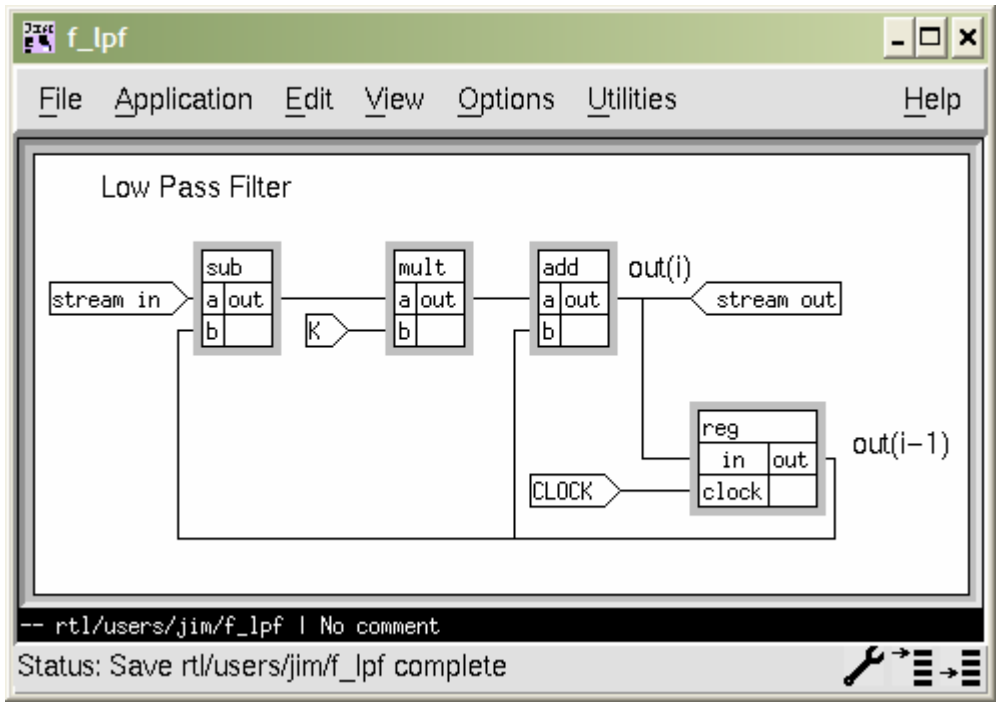
- Gedae relies on
  - C cross compilers and
  - Optimized vector libraries

  to run on DSPs.
- How do we support firmware targets like FPGAS?



Single Sample Language: Gedae-RTL

- Single sample extension to Gedae graph language
- Based on the theory of register transfer languages
- Registers store information, delayed by a clock rate

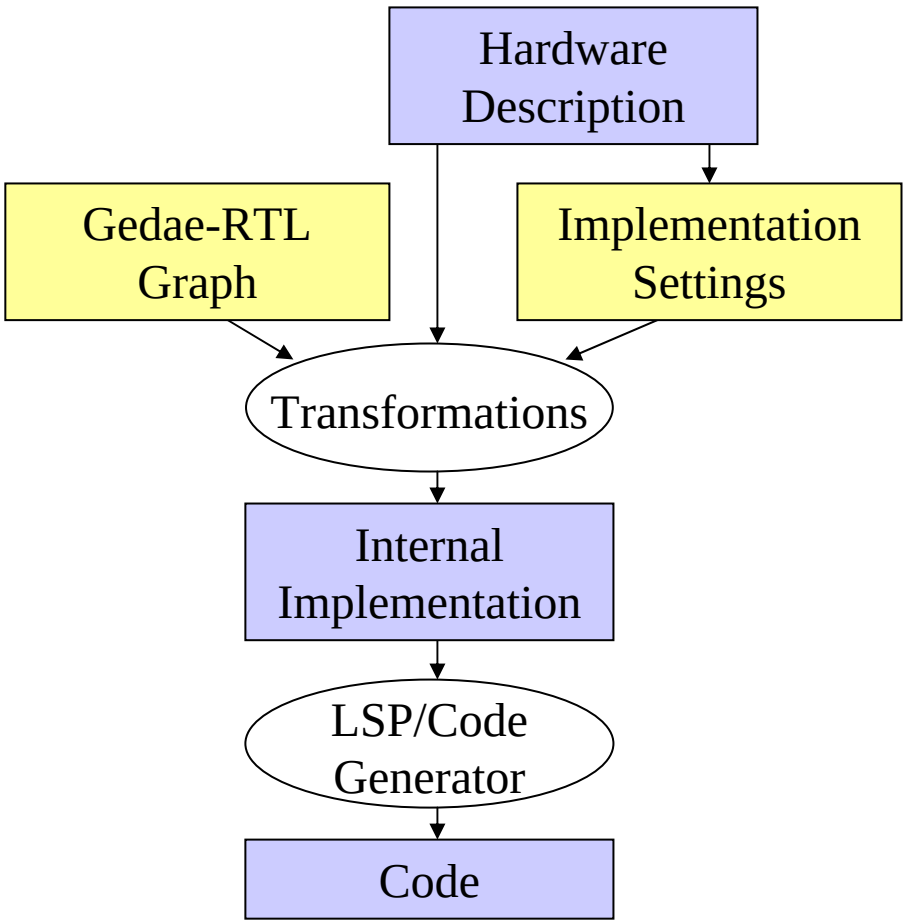



```
out(i) = K*(in(i) - out(i-1)) +
         out(i-1)
```

Gedae-RTL's Seven Functions

- Register `R(in,out,c)`
  - Copy `in` to `out` delayed by clock rate `c`.
- Assignment `A(E,out)`
  - Evaluate the expression `E` and assign its value to `out`.
- Decimate `D(in,c)`
  - Tie clock rate `c` to signal `in`.
- Clock `C(in,c)`
  - Get clock rate `c` tied to `in`.
- Memory `M(in,n,s)`
  - Allocate buffer `in` with `n` elements of size `s`.
- Read `MR(a,out)`
  - Read the element at address `a` and put the value in `out`.
- Write `MW(in,a)`
  - Write the value `in` to address `a`.

Language Independence



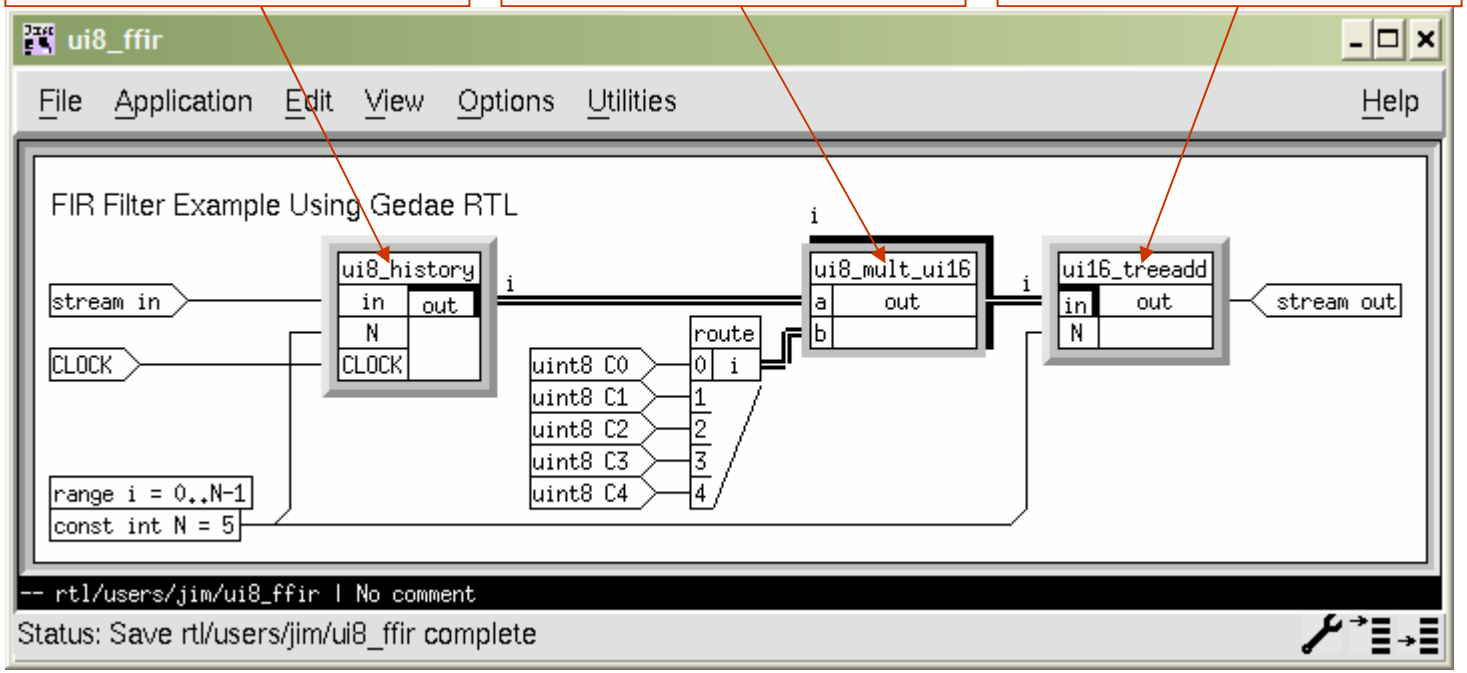
- Language Support Package (LSP) allows exportation of target-specific code
- Export Ansi-C to simulate functionality
- Export VHDL for FPGAs
- Export C enhanced for the AltiVec architecture

Example: 5-Point FIR Filter

Pipeline of N
R( ) registers

Set of N
A(a*b,out)

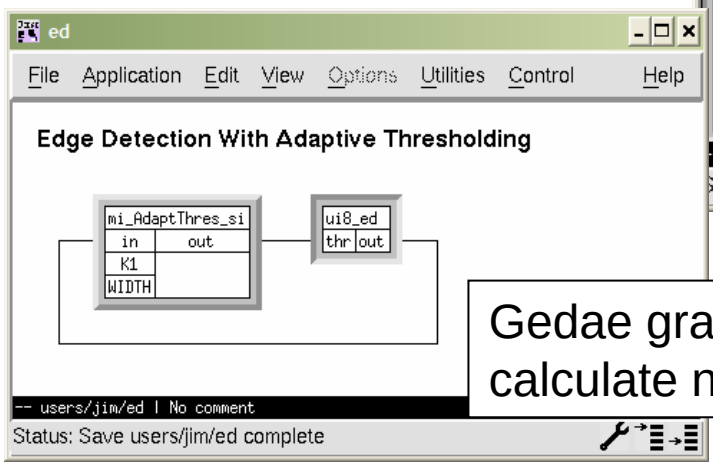
Network of N-1
A(a+b,out)



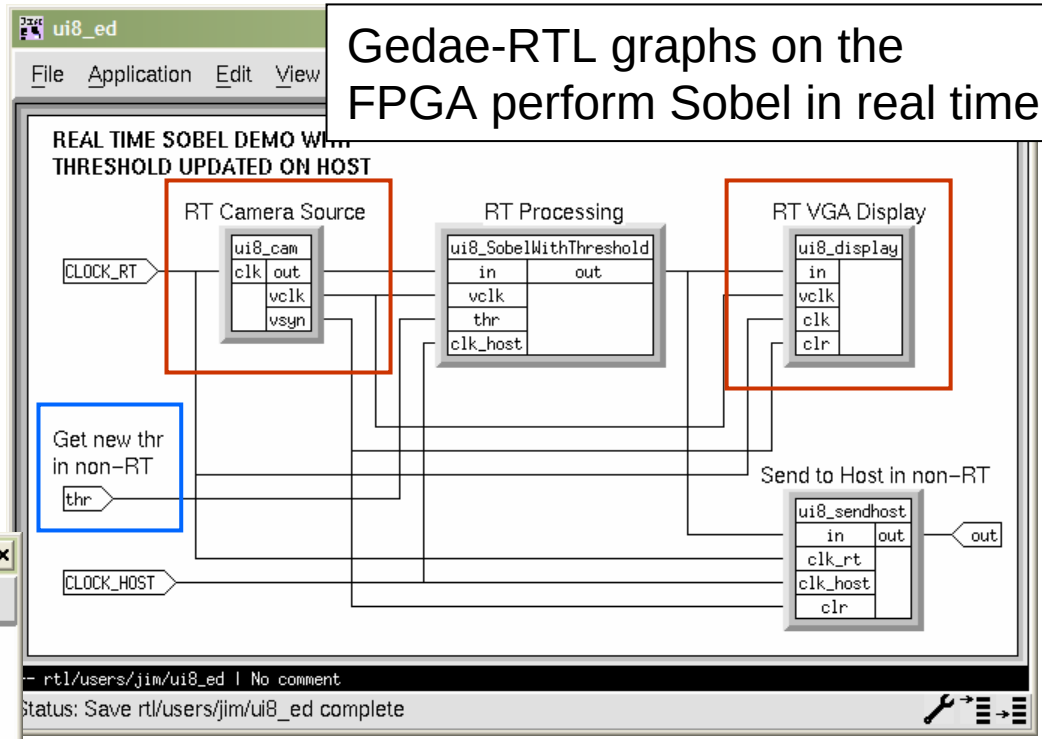

```
out(i) = C0*in(i) + C1*in(i-1) + C2*in(i-2) ...
```

Gedae Implements the Heterogeneous System

- Pin connections to camera and VGA provide real time I/O
- Host updates threshold in non-real time



Gedae graphs on the DSP calculate new thresholds



Gedae-RTL graphs on the FPGA perform Sobel in real time

Poster

Agenda

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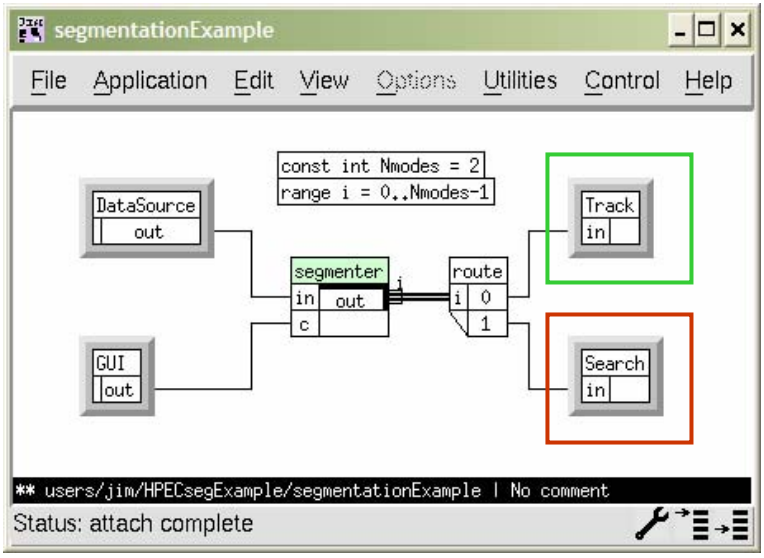
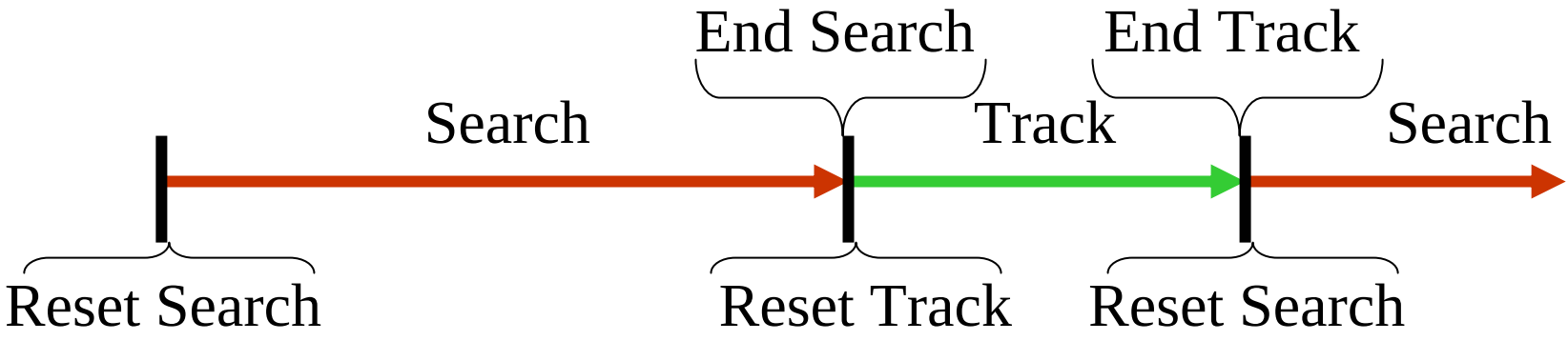
How Do We Program Modal Software in Data Flow?

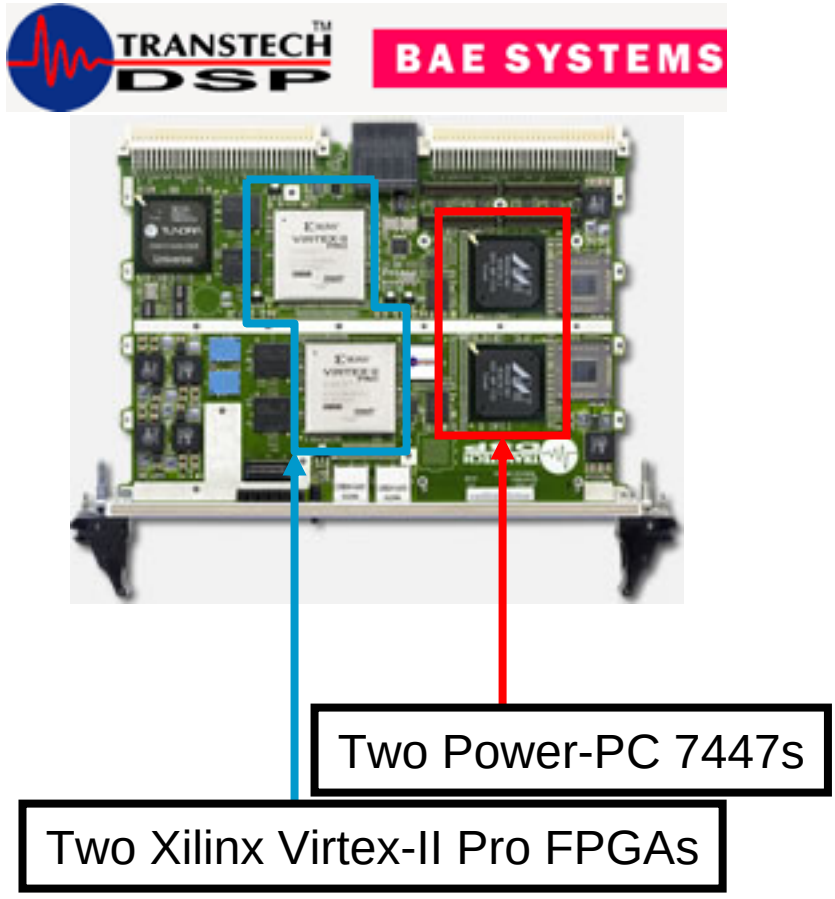


- **Modal software breaks data streams into finite length segments**
- **Extra processing at the beginning and end of segments**



How Do We Program This Heterogeneous Architecture?

- **Gedae is a powerful programming tool for boards of Power-PCs.**
- **The Gedae-RTL language extension to Gedae allows mapping processing to FPGAs.**



Gedae Language Features

Segmentation

- Reset and EndOfSegment Methods
- Exclusivity
- External State

Gedae-RTL

- Seven Functions
- Language Support Package

The Gedae language allows specification of a complete modal software system and implements it on heterogeneous hardware.